REMARKS

In the Office Action dated March 3, 2006, the Examiner has rejected claims 1-19. Applicant respectfully traverses these rejections. Applicant's traverse notwithstanding, all claims are amended. This application is based on and claims priority from earlier filed French applications. Accordingly the amendments to the claims made herein, other than those specifically mentioned below, are made only to polish the wording to conform to US practice.

Claim Rejections under 35 USC § 112

In the Office Action, the Examiner rejects claims 1 – 19 under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention, in that independent claims 1 and 17 use the vague expression "and/or" in the preamble of these claims. Additionally, the Examiner rejects claims 11-16 and 18-19 under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention, in that these dependent claims contradict their respective parent claims because these dependent claims recite that "only one of either 'duration' or 'shape' is being measured while their parent claims recite (by the use of 'and/or') that both duration and shape are included in the scope of the claims."

It is respectfully submitted that the phrase "and/or" in amended independent claims 1 and 17 has been replaced with the word "or" thereby correcting these section 112 second paragraph problems, and these claims are now allowable. As a result, dependent claims 11-16 and 18-19 are therefore allowable as well. Accordingly it is respectfully requested that these rejections under 35 USC § 112, second paragraph be withdrawn.

Claim Rejections under 35 USC § 102(e)

In the Office Action, the Examiner rejected claims 1 – 4, 10 and 17-18 under 35 USC § 102(e), as being anticipated by Hughes et al (U.S. 6,697,209), based on the assertion that "Hughes et al (6,697,209) shows, in Figure 11, a combination identical to applicant's Figure 1

(with the exception of the capacitors C_1 to C_n which are not included in claims 1-4, 10 and 17-18)." It is respectfully submitted that this Figure 11 in Hughes is also different from Applicant's Figure 1 in other ways, and that the "high resolution delay measurement circuit" depicted by Figure 11 in Hughes (see Hughes Col 4., lines 58-60) and its described use as a "fine adjustment signal generator" (see Col. 3, line 64 through Col. 4, line 7), is not the same as applicant's "electrical pulse duration or shape evaluation circuit." For example, in applicant's invention, an electric pulse may be generated in any one of the assembly of elements, contrary to the Hughes et al circuit, in which an electric pulse is always generated on the input of the first delay element. In this respect, in applicant's invention, each element has a double function: delay element and detection element generating an electric pulse in response to an external disturbance. This second function does not exist in Hughes, as explained more fully below. Accordingly, it is respectfully submitted that Hughes et al (6,697,209) does not anticipate applicant's invention and the section 102(e) rejection is therefore incorrect and should be withdrawn.

More specifically, in Hughes et al, Figure 11 is a schematic view of a "high resolution delay measurement circuit" (Col. 4, lines 58-60) for use in synchronizing the read heads of a magnetic tape drive mechanism (Col. 3, lines 3-14). This "high resolution delay measurement circuit" depicted by Hughes et al in Fig. 11 is used as a "fine adjustment signal generator" (Col. 3, line 64 to Col. 4, line 7). This "fine adjustment signal generator" generates an "adjustment signal" to compensate for the difference in "the first synchronization mark detection **time** (emphasis added) and the second synchronization mark detection **time**." (Col. 3, lines 8-14). These first and second synchronization mark detection times are the times when a synchronization mark from a tape being read by the tape drive mechanism, is detected by the first and second read heads respectively on the tape drive. (Col. 3, lines 3-8). To generate this "adjustment signal" calculated as a function of these two synchronization mark detection times, the "high resolution delay measurement circuit" depicted in Hughes et al Fig. 11 makes use of **two** (emphasis added) byte clocks (120A and 120B in Fig. 11 as described at col. 14, lines 7-9) which are used to output an indication of "delay time" (i.e. the difference between the two clocks at a given time - Col. 13, lines14-40).

On the contrary, Applicant's invention is NOT a delay time calculator, but rather a device to evaluate electronic pulses induced in an integrated circuit by an external disturbance such as a

natural radiation occurrence, and more precisely, a device to measure the duration or shape of the electronic pulse induced by the electronic disturbance (specification para 0002 and 0003). While Applicant's Figure 1 bears some similarity to Hughes et al Figure 11, it is clear that the "elements ($D_1 - D_n$)" in applicant's amended independent claim 1 may be any one of an OR gate, an AND gate, an Inverter, or any element of a cell library (para 0003, lines 21-24), and therefore are different than those shown in Hughes et al Figure 11. Moreover, Applicant's detection device in Figure 1 indicates a single clock (CLK)(para 0036, lines 29-30). Note that in Applicant's Figure 1, the input E shown is permanently set to a predetermined level (para 0037), for example level "0", and hence, is NOT a second clock as shown in Hughes et al Figure 11.

Accordingly, Hughes et al is incorrectly cited as an anticipation of applicant's invention under section 102(e) and we therefore respectfully request that the rejection under section 102(e) be withdrawn and applicant's claims passed to issue.

Applicant's amended independent claim 1 now reads as follows;

1. (Currently Amended) A circuit for evaluating duration ~~and/or~~ or shape characteristics of an electric pulse induced in an element of an integrated circuit, comprising:

an assembly of elements (D1 to Dn; d1 to dn), each element being likely to receive an occasional external disturbance generating an electric pulse in the element, wherein an element is an OR gate, an AND gate, an inverter or any element in a cell library; and

a measurement circuit (B1 to Bn, 1; b1 to bn, ~~20~~) connected to the elements to determine said characteristics of an electric pulse generated in one of the elements.

This amended independent claim 1 is now clearly distinguished over Hughes et al. Independent claim 17 has similarly been amended. Since these independent claims are now allowable, the claims which depend from these amended independent claims are also allowable and all pending claims 1-19 should be allowed and passed to issue. Applicant respectfully requests that all of these rejections be withdrawn and the claims as amended be passed to issue.

CONCLUSION

No new matter has been added. Claims 1 - 19 are currently amended. Claims 1-19 are pending and all claims now pending have been shown to be allowable. It is therefore respectfully requested that the application be passed to issue.

In the unlikely event that the transmittal letter is separated from this document and the Patent Office determines that an extension and/or other relief is required, applicant petitions for any required relief including extensions of time, and requests that the undersigned be called as soon as possible.

Respectfully submitted,

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By: _____

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